TITLE

MECHANISM FOR PREVENTING ESD DAMAGE AND LCD PANEL UTILIZING THE SAME

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to ESD protection, and in particular to a mechanism for preventing ESD damage in an electronic device.

Description of the Related Art

Fig. 1 is a schematic diagram of signal lines of a conventional liquid crystal display (LCD) panel. The LCD panel comprises a pixel array 12, a plurality of connection areas 10 and a plurality of fan-out signal lines F_1 to F_n. Integrated circuits such as a data driver and a scan driver drive the pixel array 12 to display images. As shown in Fig. 1, each connection area 10 has a plurality of pads P_1 to P_n arranged sequentially for mounting to the corresponding integrated circuit. The fan-out signal lines F_1 to F_n are extend from the pads P_1 to P_n respectively. The integrated circuits can provide driving signals, such as scan signals and data signals, to the pixel array 12 through the fan-out signal lines F_1 to F_n. Also, the integrated circuits can receive external signals through the fan-out signal lines F_1 to F_n.

A thin film transistor (TFT) LCD panel is handled by several machines and operators during the manufacturing process. When a machine or operator generates and transmits electrostatic discharge (ESD) to the TFT LCD

panel, signal lines of the TFT LCD panel are open or short, resulting in reduced yield and damage to internal elements. The resulting TFT LCD panel displays abnormal bright or dark lines. TFT LCD panels typically comprise an ESD protection device to prevent ESD from damaging the TFT LCD panel.

Referring to Fig. 1, a conventional method of protecting an LCD panel provides a plurality of ESD protection devices ES_1 to ED_n disposed corresponding to the fan-out signal lines F_1 to F_n. All the ESD protection devices usually have a virtually equal impedance. When ESD occurs in the TFT LCD panel, the ESD protection device of each signal line disposed on outermost side of the connection area 10 has the longest path. Therefore, the electrostatic charges do not disperse and the effectiveness of the protection offered by the ESD protection device is not maintained.

SUMMARY OF THE INVENTION

Accordingly, an object of the present invention is to provide a mechanism for preventing ESD damage in an electronic device, such as an LCD panel. The ESD protection devices corresponding to the longest fan-out signal lines of an integrated circuit have longer equivalent channel widths than those of the other ESD protection devices or smaller equivalent impedances than those of the other ESD protection devices.

Another object of the invention is to provide a mechanism for preventing ESD damage in an electronic device, such as an LCD panel. The ESD protection devices

corresponding to the outermost sides of the connection area have the smallest equivalent impedance and equivalent impedances of the other ESD protection devices gradually increase from the outermost sides of the connection area to the center thereof, thereby discharging the electrostatic charge efficiently.

Another object of the invention is to provide a mechanism for preventing ESD damage in an electronic device, such as an LCD panel. Any ESD protection device corresponding to one fan-out signal line of an integrated circuit has an equivalent impedance different from equivalent impedances of the other ESD protection devices, thereby discharging the electrostatic charge efficiently.

Another object of the invention is to provide an liquid crystal display panel utilizing the above mechanism for preventing ESD damages, thereby preventing the LCD panel from damaged by ESD.

A detailed description is given in the following embodiments with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention can be more fully understood by reading the subsequent detailed description and examples with references made to the accompanying drawings, wherein:

Fig. 1 is a schematic diagram of signal lines of a conventional liquid crystal display (LCD) panel.

Fig. 2 shows an example of an ESD protection device composed by a diode circuit.

Fig. 3 shows layout of the diode circuit in Fig. 2.

Fig. 4 shows an embodiment of a mechanism for preventing ESD damages in the present invention.

Fig. 5 shows another embodiment of a mechanism for preventing ESD damage in the present invention.

DETAILED DESCRIPTION OF THE INVENTION

A diode circuit is always applied to an electronic device to serve as an electrostatic discharge (ESD) protection device. The ESD protection device ES_1 shown in Fig. 2 comprises six diodes D_1 to D_6 configured corresponding to the fan-out signal line F_1 in Fig. 1. Generally, two ESD protection devices ES_1 are respectively configured at two terminals of the pad P_1, but only one is shown in Fig. 2.

The diodes D_1 to D_6 within the ESD protection devices ES_1 usually are typically composed by elements having MOS transistor circuit structures, such as a MOS transistor whose drain is coupled to its gate. Fig. 3 shows a circuit layout of diodes D_1 to D_6 in Fig. 2. As shown in Fig. 3, channel widths of the diodes D_1 to D_3 are CH1 while channel widths of the diodes D_4 to D_6 are CH2. An equivalent impedance of the ESD protection device ES_1 is determined according to the channel widths CH1 and CH2. That is, when an equivalent width composed of the channel widths CH1 and CH2 increases, the equivalent impedance of the ESD protection device ES_1 decreases.

First embodiment

Fig. 4 shows an embodiment of a mechanism for preventing ESD damage in the present invention. The mechanism is applied to an electronic device, LCD panel.

The LCD panel comprises a pixel array 12, a plurality of connection areas 10, a plurality of fan-out signal lines F_1 to F_n, and a plurality of ESD protection devices ES_1 to ED_n. Each connection area 10 has a plurality of pads P_1 to P_n arranged sequentially for mounting to one integrated circuit. The pads P_1 to P_n are disposed on two outermost sides of the connection area 10. The fan-out signal lines F_1 to F_n extend from the pads P_1 to P_n respectively. The ESD protection devices ES_1 to ED_n are disposed corresponding to the fan-out signal lines F_1 to F_n. In addition, each ESD protection device comprises a least one element having a MOS transistor circuit structure, such as a MOS transistor whose drain is coupled to its gate.

As shown in Fig. 4, equivalent impedances of the ESD protection devices ES_1 and ED_n are designed to be smaller than equivalent impedances of ESD protection devices ES_2 and ED_{n-1}. That is, an equivalent channel width L_1 of the ESD protection devices ES_1 and ED_n is designed to be longer than an equivalent channel width L_2 of ESD protection devices ES_2 and ED_{n-1}.

According to the embodiment, in one connection area 10, the equivalent impedances of the ESD protection devices ES_1 and ED_n are small, that is the equivalent channel width L_1 of the ESD protection devices ES_1 and ED_n is longest. Therefore, accumulated electrostatic charges

on the longest fan-out signal lines F_1 and F_n which do not easily disperse charges could be effectively dispersed through the ESD protection devices ES_1 and ED_n, preventing the LCD panel from ESD damage.

Second embodiment

Fig. 5 shows another embodiment of a mechanism for preventing ESD damages in the present invention. The mechanism is applied to an electronic device, an LCD panel.

The LCD panel comprises a pixel array 12, a plurality of connection areas 10, a plurality of fan-out signal lines F_1 to F_n, and a plurality of ESD protection devices ES_1 to ED_n. Each connection area 10 has a plurality of pads P_1 to P_n arranged sequentially for mounting to one integrated circuit. The pads P_1 to P_n are disposed on two outermost sides of the connection area 10. The fan-out signal lines F_1 to F_n extend from the pads P_1 to P_n respectively. The ESD protection devices ES_1 to ED_n are disposed corresponding to the fan-out signal lines F_1 to F_n. In addition, each ESD protection device comprises a least one element having a MOS transistor circuit structure, such as a MOS transistor whose drain is coupled to its gate.

As shown in Fig. 5, in one connection area 10, equivalent impedances of the ESD protection devices ES_1 to ED_n gradually increase from the ESD protection devices ES_1 and ED_n to the center of the connection area 10. That is, equivalent channel widths of the ESD protection devices ES_1 to ED_j gradually decrease and equivalent channel

widths of the ESD protection devices ES_{j+1} to ED_n sequentially increase gradually.

According to the gradual decrease in the lengths of the fan-out signal lines from the two outermost sides of the connection area 10 to the center thereof, the equivalent impedances of the ESD protection devices are designed to gradually increase. That is, the equivalent channel widths of the ESD protection devices gradually decrease from the two outermost sides of the connection area 10 to the center thereof. Therefore, electrostatic charges could be effectively dispersed through the ESD protection devices ES_1 and ED_n, preventing the LCD panel from ESD damaged.

Third embodiment

The embodiment is a mechanism for preventing ESD damages of the present invention applied to an electronic device. Among all ESD protection devices ES_1 and ED_n, an equivalent impedance of one ESD protection device ES_k $(1 \leq k \leq n)$ is different from these of the others. Each ESD protection device comprises at last one element having a MOS transistor circuit structure. Therefore, an equivalent channel width of the ESD protection device ES_k is different these of other protection devices.

While the invention has been described by way of example and in terms of the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be

accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.